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Sidewall Controlled Multistable Nematic Liquid Crystal Devices

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Bistable azimuthal nematic alignment has been produced in channels with one flat and one triangular shaped grating sidewall with a small blaze asymmetry. Two frequency addressing has been used to switch between the bistable states. It was found that the time needed to latch to the other bistable state decreases as the voltage is increased. Surface defects move towards each other along the grating sidewall during the switching pulse. If these defects annihilate before director reorientation tilt-wall loops collapse in the bulk then it is possible for the loops to move away from the surface and to collapse in the bulk of the channel.

Keywords Bistable nematic display; nematic liquid crystal; tilt-wall; two frequency material

1. Introduction

Conventional liquid crystal displays need continual electrical addressing to maintain even static images. It has been shown that bistable nematic states can retain a static image in the absence of an applied electrical field. This property gives them a potential advantage where a low update rate is required for example in e-paper, e-billboards and for smart labels and smart cards in the retail arena [1–5].

Azimuthal bistability or multistability in a nematic liquid crystal refers to a situation where two or more distinct stable alignment states of the nematic n-director are possible. For these states to remain stable when no electric field is present then there must be an energy barrier that prevents one of the states from spontaneously relaxing into the other alignment state. Methods for achieving this include patterning the substrates that contain the nematic liquid crystal with a micro-scale surface bi-grating or with nano-scale gratings [6,7], arrays of posts within the nematic layer or spanning the width of the nematic layer [2,8,9], or lateral confinement by dividing the nematic layer into square wells [8,10–12] or channels [13,14].

The current authors have previously demonstrated that using a geometry of channels with straight or patterned sidewalls it is possible to create stable azimuthal alignment states in the plane of a homogeneous layer of nematic liquid crystal. If the width of the channels is several times greater than the thickness of the layer then the

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occurrence and nature of the stable azimuthal alignment states are determined almost entirely by the morphology of the sidewalls. Previously triangular and symmetrical sidewall morphology has been investigated [13,14]. It was found that two stable alignment states were observed, but the time to switch between states was much too long to be used as a practical device. The motivation for the current paper was to investigate the effects of increasing the applied voltage on the switching times and the movement and behaviour of the defects.

2. Device Details

In the current work azimuthal bistability has been achieved by the confinement of nematic liquid crystal into channels with one flat sidewall and one grating sidewall with a triangular profile. A schematic diagram showing a section through the device is shown in Figure 1. The average channel width was $d = 80\,\mu m$ wide and the height of the channel walls, corresponding to the thickness of the liquid crystal layer, was $w = 20\,\mu m$. As the channel width to layer thickness ratio is kept small the nematic **n**-director remains in the x-y plane and the nature of the sidewall geometry determines the alignment states within the device. The period of the grating sidewall was $p = 80\,\mu m$ and the triangular profile grating amplitude was $a = 20\,\mu m$. There was a small blaze asymmetry of the triangular shaped walls in which the peaks were moved in one direction towards the troughs by 4 μm blaze to give a small bias to the switching direction.

The substrate of the device is a glass slide of thickness 1.1 mm that had been pre-coated with indium tin oxide (ITO) of sheet resistance 50 Ohms/square. ITO inter-digitated electrodes with finger and spacing dimensions of 120 μm were used. To produce the electrodes, firstly the photo-resist S1813 was spun onto the substrate at 2000 rpm for 30 seconds resulting in a uniformly flat layer of 2 μm thickness. The sample was then exposed to 1.4 seconds of U.V light of 51.6 mW/cm^2 through a chrome/quartz photomask. After developing, the unwanted ITO was then removed by etching the sample in 1 M oxalic acid for 15 mins.

SU8 photo-resist was used for the dielectric layers and wall structures within the device. SU8 is an epoxy based negative photo-resist that can be used to fabricate thick patterns with smooth walls which is strong, stiff and chemically resistant after processing. It is suited for this application where permanent structures made from the cured material are in contact with liquid crystal material. The dielectric surface layers were formed by spinning the SU8 onto the ITO electrodes at 3000 rpm for 30 seconds producing a 2 μm layer of SU8 photo-resist. This layer was then exposed to

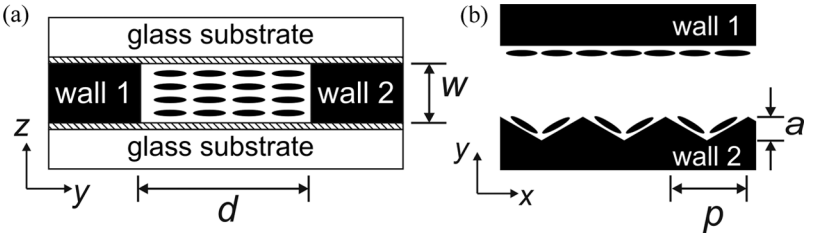

Figure 1. The device geometry. (a) Shows the plan view of the device and (b) shows the side view of the device.

UV light for 20 seconds and heated up to 115°C to fully cure the SU8. Arrays of channels were then fabricated from SU8 onto the dielectric layer. SU8 25 was spun on at 500 rpm for 5 seconds and then at 3000 rpm for 30 seconds to produce a uniform layer of 20 μm thick. The sample was then exposed to 36 seconds of U.V light of 26.0 mW/cm^2 through a chrome/quartz photo-mask. Unwanted material was removed by immersing the device in SU8 developer solution. The SU8 material on the substrate was then hardened by baking for 5 mins at 115°C.

A second glass substrate was then coated with a 2 μm layer of SU8 and placed into contact with the channels before the heating stage of the photolithography process. After completion of the photo-lithographic process the top glass substrate is chemically bonded to the top of the channels. The devices then consists of a glass substrate with ITO electrodes, a 2 μm dielectric layer of SU8, SU8 patterned channels, a second 2 μm dielectric layer of SU8 and finally a glass top as shown in Figure 1.

After assembly the commercial liquid crystal MLC2048 (Merck) was drawn in its isotropic phase into the channels by capillary action. The complete device was heated to 80°C, so that the liquid crystal material was above its isotropic-nematic phase transition, and then cooled slowly at 0.5°C per minute to room temperature. The liquid crystal MLC2048 (Merck) exhibits a positive dielectric constant at low frequencies and a negative dielectric constant at high frequencies, with a cross over frequency of 20 kHz. When an A.C sinusoidal waveform is applied to the electrodes under the channel walls it is possible to align the liquid crystal parallel with the field direction (perpendicular to the channels) with low frequency of 1 kHz and perpendicular to the field direction (parallel to the channels) with a high frequency of 100 kHz.

3. Optical Textures of Static Bistable Alignment States

Figure 2 shows the theoretical 2-dimensional n-director alignment configurations in the 4 μm blazed triangular structures [14]. In these Figures the solid lines indicate the direction of the **n**-director orientations at different x-y position in the device. The director angle at the surface of the sidewalls is constrained to align in the plane of the surface. There are two distinct director alignments possible with the geometry of the sidewalls. The alignment state in Figure 2(a) is where the liquid crystal aligns horizontal at the flat sidewall and substantially horizontal in the grooves at the triangular sidewall and will be referred to as a "planar" state. The second state as seen in Figure 2(b) is where the liquid crystal aligns horizontal at the flat sidewall and

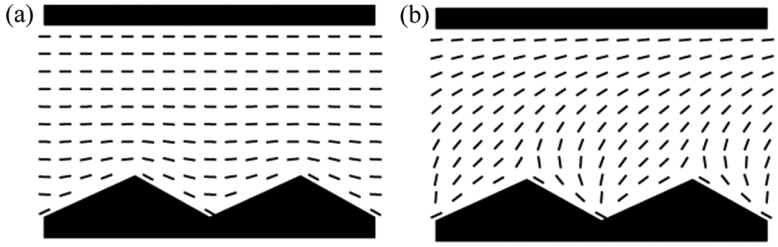

Figure 2. Theoretical 2-dimensional director alignment configurations: (a) a planar state and (b) a HAN state (figure courtesy of A.J. Davidson, reproduced with permission).

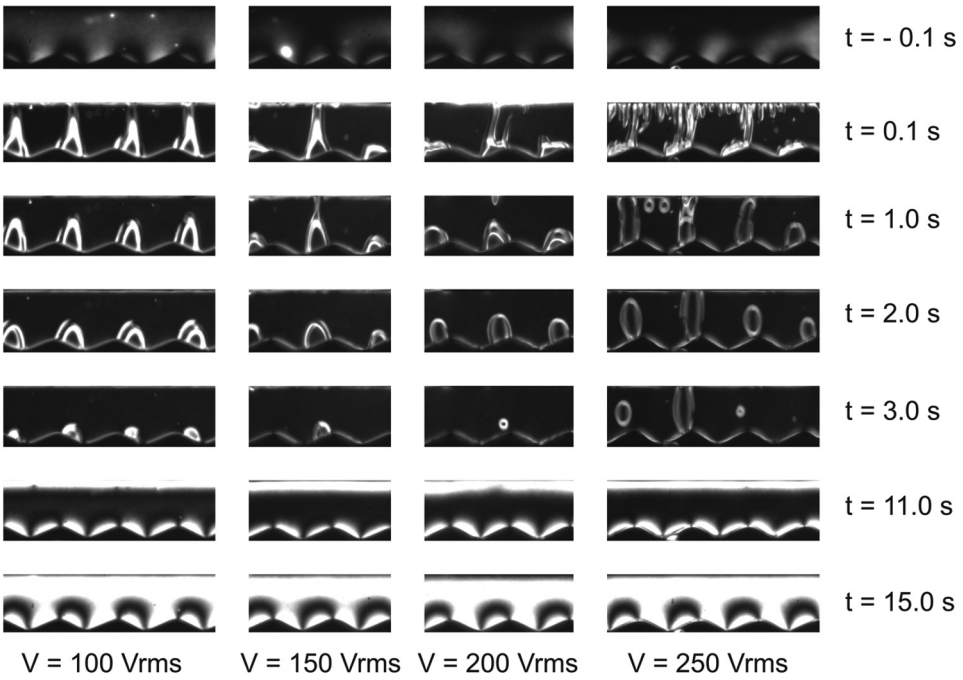

Figure 3. Experimental optical textures for switching from the planar state to the HAN state with a 1 kHz sine wave with an applied voltage (r.m.s.) of (a) 100 V, (b) 150 V, (c) 200 V and (d) 250 V. The voltage was applied at $t = 0.0$ seconds and terminated at $t = 10.0$ seconds.

substantially vertical in the grooves at the triangular sidewall and this will be referred to as a "HAN" state. The HAN nomenclature is used as an analogy with the Hybrid Aligned State observed when a layer of nematic liquid crystal is sandwiched between one plate that imparts planar surface anchoring and one plate that imparts homeotropic surface anchoring.

Experimental optical textures were recorded in transmission using a polarising optical microscope with a magnification of 500×. In Figure 3, each column shows the optical textures for the switching from a planar state to a HAN state in response to a 1 kHz r.m.s. voltage of (a) 100 V, (b) 150 V, (c) 200 V and (d) 250 V. The 1 kHz voltage waveform was applied at $t = 0.0$ seconds and terminated at $t = 10.0$ seconds. Once the voltage was applied a director reorientation tilt-wall loop forms and the surface defects at the end of the loop move towards each other along one facet of the grating. The loop area reduces as a function of time [14]. It was found in the current study that as the voltage was increased the speed that the defects move along the surface increases and it can be seen that at high voltages (200 V and 250 V) the defects can meet and annihilate before the loop has closed. Under these circumstances the loop moves away from the surface and closes in the bulk of the channel.

In Figure 4, each column shows the optical textures for the switching from a HAN state to a planar state in response to a 100 kHz r.m.s. voltage of (a) 100 V, (b) 150 V, (c) 200 V and (d) 250 V. The 100 kHz voltage waveform was applied at $t = 0.0$ seconds and terminated at $t = 10.0$ seconds. As with the planar to HAN switching, once the voltage was applied a director reorientation tilt-wall loop forms

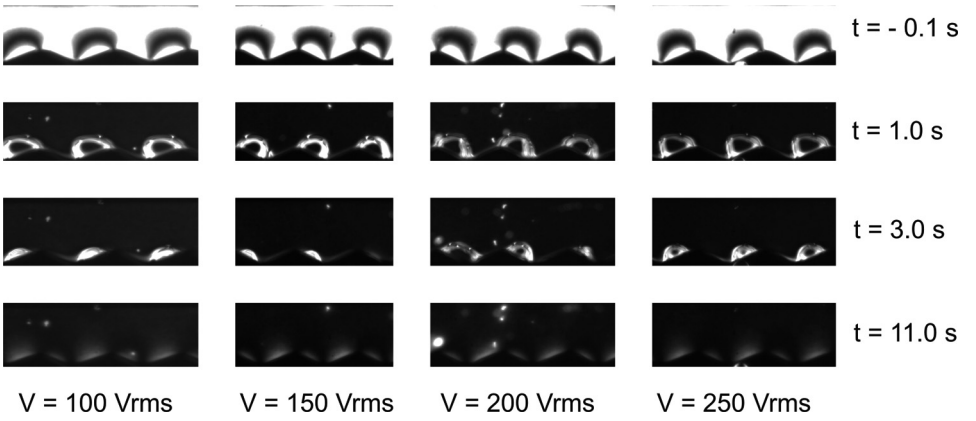

Figure 4. Experimental optical textures for switching from the HAN state to the planar state with a 100 kHz sine wave with an applied voltage (r.m.s.) of (a) 100 V, (b) 150 V, (c) 200 V and (d) 250 V. Voltage applied at $t = 0.0$ seconds and terminated at $t = 10.0$ seconds.

and the surface defects at the end of the loop move towards each other along one facet of the grating. However, for the HAN to planar switching in Figure 4 there is very little difference in the size and shapes of the loops as a function of voltage.

4. Defect Position and Loop Diameter

In Figures 5 and 6 the position of the defects $z_1(t)$ and $z_2(t)$ on the surface (relative to the facet along which they move) and the effective loop diameter are shown as a function of time. The effective loop diameter $d(t)$ was calculated from the loop area $A(t)$ using the relationship $d(t) = \sqrt{4A(t)/\pi}$. This normalisation was carried out simply so that two quantities with the dimension distance can be compared. Figure 5 shows data for switching from a planar state to a HAN state in response to a 1 kHz r.m.s. voltage, and Figure 6 shows data for the switching from a HAN state to a planar state in response to a 100 kHz r.m.s. voltage where the r.m.s. voltages in each case were (a) 100 V, (b) 150 V, (c) 200 V and (d) 250 V.

Figures 5 and 6 show data for two distinct periods on the triangular grating. For planar to HAN switching the loop closes at 6.3 ± 0.3, 4.5 ± 0.3, 4.0 ± 0.3, and 3.0 ± 0.5 seconds and the defects meet at 8.0 ± 0.3, 4.8 ± 0.3, 4.0 ± 0.3 and 2.5 ± 0.5 seconds for 100 V, 150 V, 200 V and 250 V respectively. These are the averages of the values for the two distinct periods. Both of these times decrease as the voltage is increased. At both 100 V and 150 V the loop closes before the defects meet. At 200 V the defects meet on average at the same time as the loop closes, but at 250 V the defects meet on average before the loop closes and so the loop moves into the bulk of the channel. For HAN to planar switching the loop closes at 3.5 ± 0.3, 3.0 ± 0.3, 2.8 ± 0.3, and 2.5 ± 0.3 seconds and the defects meet at 4.3 ± 0.3, 3.5 ± 0.3, 3.0 ± 0.3, and 2.8 ± 0.3 seconds for 100 V, 150 V, 200 V and 250 V respectively. In this switching direction the loops always close before the defects move together and annihilate and so the final part of the switching involves the defects coming together along the wall separated by a director reorientation tilt-wall line.

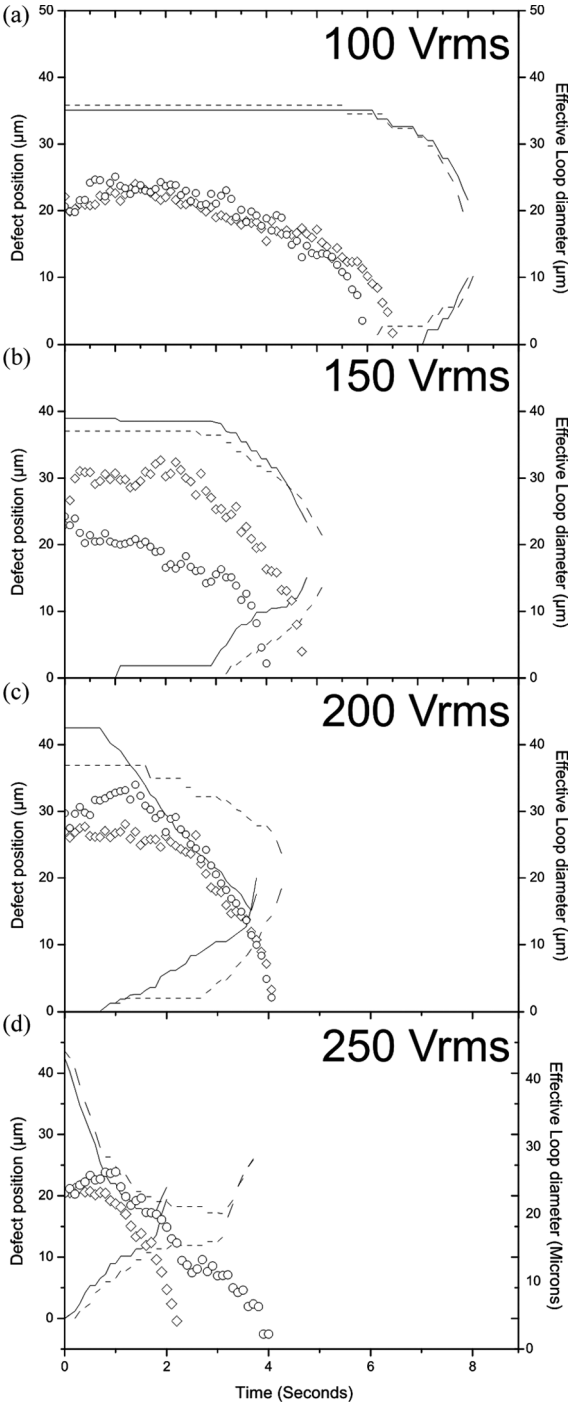

Figure 5. The position of defects along the grating sidewall and the effective loop diameter during switching from planar state to HAN state with an applied voltage (r.m.s.) of (a) 100 V, (b) 150 V, (c) 200 V and (d) 250 Vrms. Data is shown for two distinct periods closing where the continuous and dashed lines are the position of defects and the circles and diamonds are the effective loop diameters for each of the two periods.

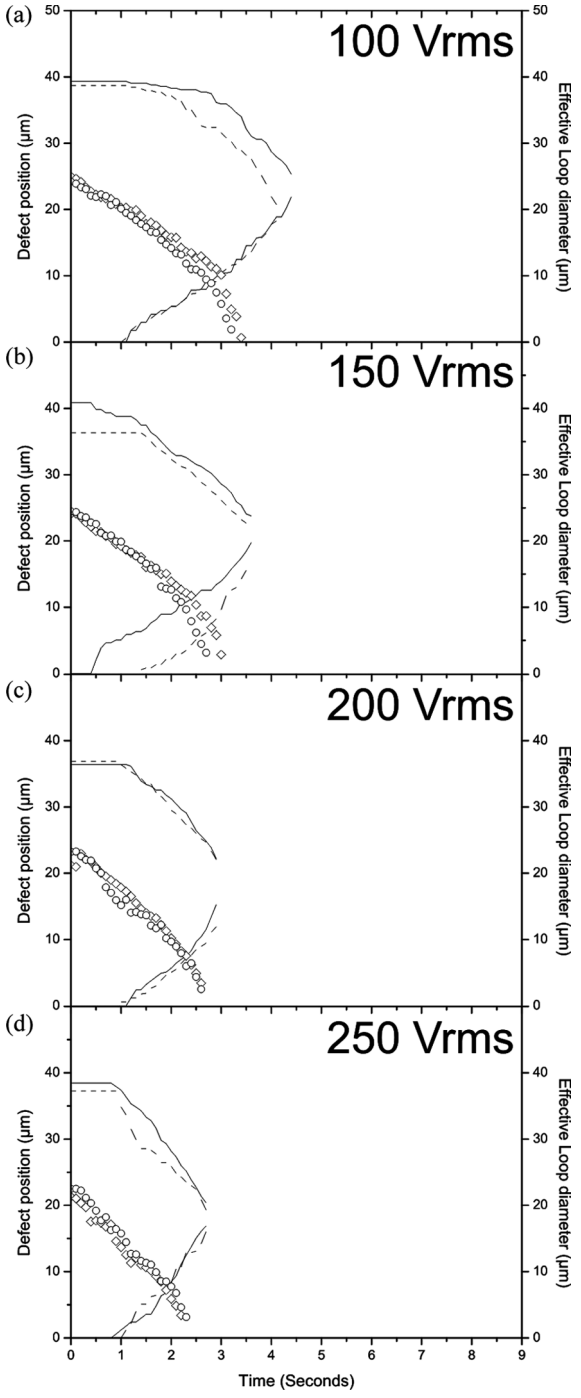

Figure 6. The position of defects along the grating sidewall and the effective loop diameter during switching from the HAN state to planar state with an applied voltage (r.m.s.) of (a) 100 V, (b) 150 V, (c) 200 V and (d) 250 V. Data is shown for two distinct periods closing where the continuous and dashed lines are the position of defects and the circles and diamonds are the effective loop diameters for each of the two periods.

5. Conclusion and Discussion

Switching between two stable alignment states in a channel bounded by a flat wall and a triangular profile grating sidewall has been observed and the time dependent movement of the surface defects and collapsing of director reorientation tilt-wall loops measured. It has been shown that it is possible to switch from the planar alignment state to the HAN alignment state and vice versa and that the time required to switch between the states reduces monotonically as the voltage is increased. It has also been found that by increasing the applied voltage it is possible to make the defects move together and annihilate before the loop has closed when switching from planar to HAN alignment state. This has resulted in the loop leaving the surface of the sidewalls and closing in the bulk of the nematic liquid crystal.

For a practical device it would be necessary to considerably reduce both the switching time and the magnitude of the applied voltage. Two possible approaches towards achieving these reductions include decreasing the width of the channel and bringing the electrodes closer together, and reducing the pitch and amplitude of the surface grating. Smaller electrode gaps will increase the electric field intensity and thus reduce the required voltage, and smaller grating features will decrease the distance travelled by the surface defects and potentially reduce the latching time.

Acknowledgment

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References

[1] Dozov, I., Nobili, M., & Durand, G. (1997). *Appl. Phys. Lett.*, *70*, 1179.
[2] Kitson, S., & Geisow, A. (2002). *Appl. Phys. Lett.*, *80*(19), 3635.
[3] Bryan-Brown, G. P., Brown, C. V., & Jones, J. C. UK Patent GB2318422, 16 Oct 1995.
[4] Brown, C. V., Towler, M. J., Hui, V. C., & Bryan-Brown, G. P. (2000). *Liq. Cryst.*, *27*, 233.
[5] Yang, D.-K., West, J., Chien, L.-C., & Doane, J. W. (1994). *J. Appl. Phys.*, *76*, 20.
[6] Kim, J.-H., Yoneya, M., & Yokoyama, H. (2002). *Nature*, *420*, 159.
[7] Bryan-Brown, G. P., Towler, M. J., Bancroft, M. S., & McDonnell, D. G. UK patent GB2286467, 8 Feb 1995.
[8] Thurston, R. N., Cheng, J., & Boyd, G. D. (1980). *IEEE Trans. Elec. Dev.*, *ED27*(11), 2069.
[9] Majumdar, A., Newton, C. J. P., Robbins, J. M., & Zyskin, M. (2007). *Phys. Rev. E*, *75*, 051703.
[10] Mottram, N. J., Ramage, A., Kelly, G., & Davidson, A. J. UK patent GB20040026582, 8th June 2006.
[11] Tsakonas, C., Davidson, A., Brown, C. V., & Mottram, N. J. (2007). *Appl. Phys. Lett.*, *90*, 111913.
[12] Wells, G. G., & Brown, C. V. (2007). *Appl. Phys. Lett.*, *91*, 223506.
[13] Ladak, S., Davidson, A., Brown, C. V., & Mottram, N. J. (2009). *J. Phys. D: Appl. Phys.*, *42*, 85114–85121.
[14] Davidson, A. J., Brown, C. V., Mottram, N. J., Ladak, S., & Evans, C. R. (2010). *Phys. Rev. E*, *81*(5), 051712.